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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,021	07/26/2001	Chien-Ping Huang	71987-10000	8130

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	09/916,021	HUANG ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears n the c ver sheet with th correspond nce address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on May 2, 2002 has been received and entered in the case.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 ~ 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 12, it cannot be determined what the applicant regards as the "wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound." That is, the limitation "wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant" eliminates the encapsulant or the molding compound from the interface layer. Therefore, there is no adhesion between the interface layer and the molding compound, hence the claim cannot be understood.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 2, 4, 6, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al.

Regarding claim 1, Johnson et al. discloses in Figs. 15 and 16 a semiconductor package with a heat sink, comprising:

- a chip carrier (12);
- at least one chip (14) mounted on the chip carrier (12) and electrically connected to the chip carrier (see Figs. 15 and 16);
- a heat sink (40) having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface

(see Figs. 15 and 16), wherein the first surface of the heat sink is attached to the chip for interposing the chip between the chip carrier and the heat sink (see Figs. 15 and 16);

- an interface layer (41, the top) formed on the second surface of the heat sink; and
- an encapsulant (24) made of the molding compound for encapsulating the chip and filling a gap between the first surface of the heat sink and the chip carrier (see Figs. 15 and 16), wherein the interface layer (41, the top) and the side surfaces of the heat sink (40) are exposed to outside of the encapsulant (see Figs. 15 and 16), and the side surfaces of the heat sink (40) are in a coplane with side edges of the encapsuiant (24 and see Figs. 15 and 16).

Further, Johnson et al. discloses the limitation "wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound" since there is no encapsulant material contacting the interface layer (41, the top).

Regarding claim 2, note Figs. 15 and 16 of Johnson et al., where he/she shows wherein the heat sink has a surface area dimensionally same as that of the chip carrier (see Figs. 15 and 16).

Regarding claim 4, note Figs. 15 and 16 of Johnson et al., where he/she shows wherein the chip carrier is a substrate (see Figs. 15 and 16; read column 3, line 29).

Regarding claim 6, note Figs. 15 and 16 of Johnson et al., where he/she shows wherein the chip is electrically connected to the substrate through solder bumps (see Figs. 15 and 16).

Regarding claim 9, since Johnson et al. does not disclose grinding the surface of the heat sink, the surface thereof is inherently roughened, corrugated or made uneven.

Regarding claim 10, note Figs. 15 and 16 of Johnson et al., where he/she shows wherein at a position on the first surface of the heat sink corresponding to the chip (14) there is formed a connecting portion (41, the bottom) extending toward the chip (14) for connecting the heat sink (40) to the chip (14) through the connecting portion (see Fig. 16), while the first surface of the heat sink (40) other than the position of the connecting portion being spaced from the chip (see Fig. 16).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Karnezos.

Johnson et al. discloses the claimed invention except wherein the interface layer on the second surface of the heat sink is made of a material selected from a group consisting of gold, chromium, nickel, alloy thereof or Teflon. However, Karnezos discloses wherein the interface layer on the second surface of the heat sink is made of a material selected from a group consisting of gold, chromium, nickel, alloy thereof or Teflon (read column 12, lines 35 ~ 40).

Johnson et al. and Karnezos are analogous art because they are from the same field of endeavor, that is the semiconductor device. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use nickel as a material for the interface layer of Karnezos with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to provide an electrically conductive surface (column 12, lines 39 ~ 40). Therefore, it would have been obvious to combine Johnson et al. with Karnezos to obtain the invention as specified in claim 3.

Regarding claim 11, a further difference between Johnson et al. and claimed invention is wherein the heat sink is attached to the chip through a thermally conductive adhesive. However, Karnezos discloses wherein the heat sink is attached to the chip through a thermally conductive adhesive (113 in Fig. 3A and read column 7, lines 61 ~ 65). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the thermally conductive adhesive of Karnezos with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to increasing bond strength between the heat sink and the chip. Therefore, it would have been obvious to further combine Johnson et al. with Karnezos to obtain the invention as specified in claim 11.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of DiStefano.

Johnson et al. discloses the claimed invention except wherein the chip is electrically connected to the substrate through bonding wires. However, DiStefano discloses wherein the chip is electrically connected to the substrate through bonding wires (54 in Fig. 1; read column 7,

lines 44 ~ 46). Johnson et al. and DiStefano are analogous art because they are from the same field of endeavor, that is the semiconductor device. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include bonding wires of DiStefano with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to reducing heat between chip and substrate. Therefore, it would have been obvious to combine Johnson et al. with DiStefano to obtain the invention as specified in claim 5.

9. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Huang et al.

Johnson et al. discloses the claimed invention except wherein the chip carrier is a QFN (quad flat nonlead) lead frame and wherein the chip is electrically connected to the QFN lead frame through bonding wires. However, Huang et al. discloses wherein the chip carrier is a QFN (quad flat nonlead) lead frame (see Figs. 1 ~ 7 and read column 3, lines 30 ~ 31) and wherein the chip is electrically connected to the QFN lead frame through bonding wires (216 in Fig. 6 and 316 in Fig. 7). Johnson et al. and Huang et al. are analogous art because they are from the same field of endeavor, that is the semiconductor device. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the QFN (quad flat nonlead) lead frame and the bonding wires of Huang et al. with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to improve the heat-dissipating effect of the package (column 2, lines 8 ~ 10). Therefore, it would have been obvious to combine Johnson et al. with Huang et al. to obtain the invention as specified in claims 7 and 8.

10. Claims 12, 13, 15, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Lai et al.

Johnson et al. discloses the claimed invention except at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip. However, Lai et al. discloses at least one buffer pad (5) attached to the chip (3) and made of a material having a similar thermal expansion coefficient to the chip (see Fig. 2 and read column 4, lines 52 ~ 67). Johnson et al. and Lai et al. are analogous art because they are from the same field of endeavor, that is the semiconductor device. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include at least one buffer pad of Lai et al. with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to prevent thermal compressive stress and tensile stress resulted from the encapsulant during packaging process (column 3, lines 1 ~ 7). Therefore, it would have been obvious to combine Johnson et al. with Lai et al. to obtain the invention as specified in claim 12.

Further, Johnson et al. discloses the limitation "wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound" since there is no encapsulant material contacting the interface layer (41, the top).

Regarding claim 13, note Figs. 15 and 16 of Johnson et al., where he/she shows wherein the heat sink has a surface area dimensionally same as that of the chip carrier (see Figs. 15 and 16).

Regarding claim 15, note Figs. 15 and 16 of Johnson et al., where he/she shows wherein the chip carrier is a substrate (see Figs. 15 and 16; read column 3, line 29).

Regarding claims 16 and 20, a further difference between Johnson et al. and claimed invention is wherein the chip is electrically connected to the substrate through bonding wires and wherein the heat sink is attached to the buffer pad through a thermally conductive adhesive. However, Lai et al. discloses wherein the chip (3 in Fig. 2 of Lai et al.) is electrically connected to the substrate (2 in Fig. 2 of Lai et al.) through bonding wires (8 in Fig. 2 of Lai et al.) and wherein the heat sink (4a in Fig. 3 of Lai et al.) is attached to the buffer pad (5a in Fig. 3 of Lai et al.) through a thermally conductive adhesive (6a in Fig. 3 of Lai et al.; read column 5, lines 6 ~ 9 and column 6, lines 50 ~ 56). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to further include the bonding wires and the thermally conductive adhesive of Lai et al. with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to further prevent thermal compressive stress and tensile stress resulted from the encapsulant during packaging process (column 6, lines 53 ~ 56). Therefore, it would have been obvious to further combine Johnson et al. with Lai et al. to obtain the invention as specified in claims 16 and 20.

Regarding claim 19, since Johnson et al. does not disclose grinding the surface of the heat sink, the surface thereof is inherently roughened, corrugated or made uneven.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Lai et al. as applied to claim 12 above, and further in view of Karnezos.

Johnson et al., as modified, discloses the claimed invention except wherein the interface layer on the second surface of the heat sink is made of a material selected from a group consisting of gold, chromium, nickel, alloy thereof or Teflon. However, Karnezos discloses

wherein the interface layer on the second surface of the heat sink is made of a material selected from a group consisting of gold, chromium, nickel, alloy thereof or Teflon (read column 12, lines 35 ~ 40). Johnson et al., as modified, and Karnezos are analogous art because they are from the same field of endeavor, that is the semiconductor device. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to further include the nickel as a material for the interface layer of Karnezos with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to provide an electrically conductive surface (column 12, lines 39 ~ 40). Therefore, it would have been obvious to further combine Johnson et al. with Karnezos to obtain the invention as specified in claim 14.

12. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Lai et al. as applied to claim 12 above, and further in view of Huang et al.

Johnson et al., as modified, discloses the claimed invention except wherein the chip carrier is a QFN (quad flat nonlead) lead frame and wherein the chip is electrically connected to the QFN lead frame through bonding wires. However, Huang et al. discloses wherein the chip carrier is a QFN (quad flat nonlead) lead frame (see Figs. 1 ~ 7 and read column 3, lines 30 ~ 31) and wherein the chip is electrically connected to the QFN lead frame through bonding wires (216 in Fig. 6 and 316 in Fig. 7). Johnson et al. and Huang et al. are analogous art because they are from the same field of endeavor, that is the semiconductor device. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to further include the QFN (quad flat nonlead) lead frame and the bonding wires of Huang et al. with the semiconductor device of Johnson et al. The suggestion or motivation for doing so would have been to improve the heat-

dissipating effect of the package (column 2, lines 8 ~ 10). Therefore, it would have been obvious to further combine Johnson et al. with Huang et al. to obtain the invention as specified in claims 17 and 18.

Response to Arguments

13. Applicant's arguments filed on May 2, 2002 have been fully considered but they are not persuasive.

Applicant argues "Johnson fails to teach or suggest a semiconductor package having an interface layer formed on a heat sink, wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound." The argument is not persuasive. Johnson discloses in Figs. 15 and 16a semiconductor package having an interface layer (41, the top) formed on a heat sink (40), wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound since no molding compound contacts the interface layer.

For the above reason the rejection is maintained.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Chris C. Chu
Examiner
Art Unit 2815

c.c.
July 9, 2002